ABSTRACT

A Flash memory that stores data, code, and parameters and performs parallel operations employs uniform-size blocks in array planes. The Flash memory includes separate internal read and write paths connected to multiple array planes to permit a read in one array plane during a write in another array plane, further a third array plane can erase a block during the read and write operations. The uniform size, which permits a symmetric layout, is selected for efficient storage of parameters to provide maximum flexibility in allocation of storage. A redundancy system for the Flash memory uses a CAM and a RAM for address comparison and substitution when replacing addresses corresponding to defective memory elements. The uniform block size allows block replacement where spare blocks in the array planes replace defective blocks. To reduce access delays from signal propagation through the CAM and RAM, part of the input address such as the row address goes directly to decoders while another part of the input address such as the block address goes to the CAM array for comparison.